Exhibit A

(Bhardwaj et al Declaration)

Single-Factor Analysis f Simulated Stress-Induced Birefringence in Scion AWG Devices

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Introduction

Birefringence is a common problem in PLC arrayed waveguides (AWGs) and one that we have observed in our first devices as a measured passband split between TE and TM polarizations. Since polarization dependent device performance is not acceptable for fiber optic transmission applications, measures must be taken to eliminate it. Controlling birefringence means controlling the stress fields created in the waveguide cores during PLC fabrication. Hence, we have begun to explore the first of several options available to us – stress relief grooves (SRG). Simulation has been used to evaluate the stress characteristics of our base AWG device and then to refine SRG design parameters. This report summarizes the results of the most recent work.

Birefringence and Stress

Birefringence is caused by the difference in stress exerted on the waveguide *normal* to the wafer surface and that exerted across its width (*transverse*). These stresses are a combination of internal film stress formed in the PSG cores when they are cooled following anneal and external stresses imposed by the surrounding thermal oxide and BPSG clad films. The birefringence, **B**, in the waveguide cores is related to the stress by:

$$\mathbf{B} = n_{TE} - n_{TM} = -(B_2 - B_1)(\sigma_{yy} - \sigma_{xx})$$

where n_{TE} & n_{TM} are the normal and transverse mode refractive indices, σ_{yy} & σ_{xx} are the normal and transverse oriented components of the stress tensor, and B_2 & B_1 are the stress optic coefficients relating the two. By computing the stress for a portion of the AWG structure, birefringence in the waveguide cores can be accurately estimated. Furthermore, modifications to the AWG structure can be evaluated for their ability to reduce or eliminate polarization dependence.

Base AWG Structure

Initial simulations were run on a model that conformed to the actual first-wafer structures fabricated on 6" wafers via the Scion virtual line. Acceptable agreement was obtained between predicted and measured passband split data for both base and SRG modified structures. This validation of the approach and its implementation allows us to now use the model as a design evaluation tool. As a starting point for such a study, a preliminary set of specifications was assembled for the base structure (see Table 1). Note that the nominal clad thickness may undergo further adjustment, so the stated "spec" represents the range of values being considered. Also note that the core spacing varies across the waveguide array and from design to design, so this "spec" covers the range of spacings for the current design. Figure 1 shows a 2-D cross-section of the 3-D model geometry for

a single waveguide in the nominal base structure. The full structure used in the simulations includes the silicon wafer, the bottom thermal oxide layer, and covers nine waveguides that are each 300 μm long.

Table 1: Preliminary specifications for the base AWG PLC structure.

Design Parameter	Nominal	Specification
Core Thickness	6.0 μm	± 0.2 μm
Core Width	6.0 μm	± 0.2 μm
Core Sidewall Angle	88.0 °	± 1.0 °
Core Overetch	0.75 μm	± 0.25 μm
Core Spacing*	23.0 μm	± 5.0 μm
Clad Thickness**	15.0 μm	± 3.0 μm

* Varies across array and from design to design; range represents typical values.
** Measured from the top of the core; final design value yet-to-be-determined; range represents possible values.

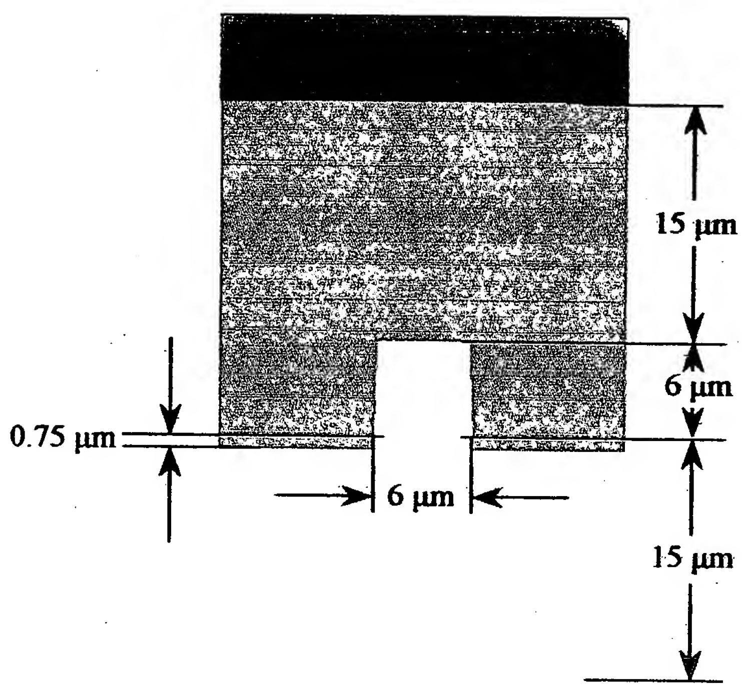

Figure 1: Nominal base design for the AWG PLC structure.

AWG Structure with SRG

Similar specification estimates were assembled for critical SRG trench parameters (see Table 2). Since SRG design is still largely an open question, these are starting nominal values with large ranges suitable for analysis and process development. Note that "Remaining Clad" refers to the distance from the bottom of the etched SRG trench to the top of the thermal oxide buffer layer *before* it has been overetched during core formation; negative values mean that the trench is below the original top of the buffer layer. Figure 2 shows a perspective view of the model geometry for this case, which is just the nominal base case plus the nominal SRG trench structure.

Table 2: Preliminary specifications for the AWG SRG structure.

Design Parameter	**Nominal**	**Specification**
Remaining Clad*	-0.375 μm	± 0.375 μm
Trench Width**	5.5 μm	± 1.0 μm
Trench Sidewall Angle	85.0 °	± 2.0 °
Trench Alignment Offset***	0.0 μm	± 0.5 (1.0) μm

* Measured relative to buffer layer top before overetch.
** Measured at the top; design feature with final value yet-to-be-determined.
*** Since effect is symmetric (-0.5 μm result = +0.5 μm result), 0.5 μm and 1.0 μm were simulated to gain added insight.

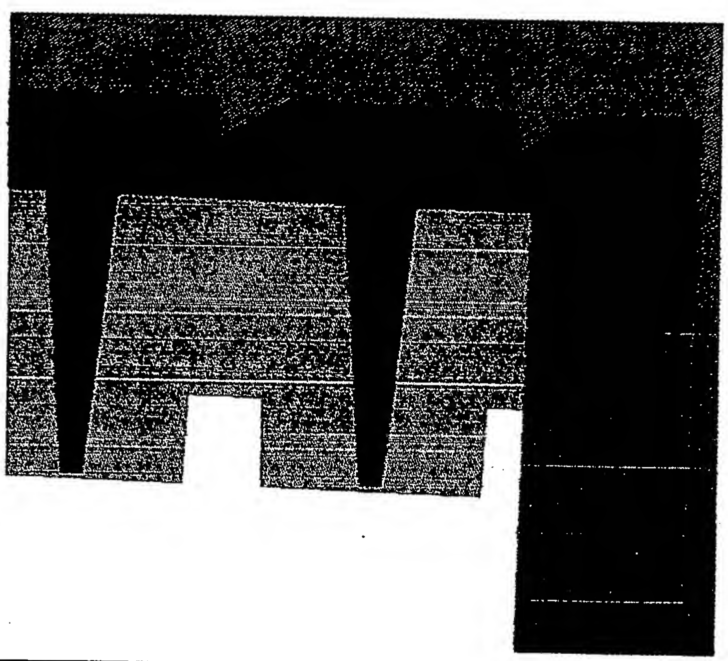

Figure 2: Preliminary nominal design for the AWG SRG structure.

Base AWG Simulati n Results

Simulations were run for the nominal base case and then for each end of the specification range shown in Table 1. The results are plotted in Figure 3 over a range of –1 to +1 indicating the normalized range for each variable. Birefringence values (RI shifts) are shown along with the expected split in TE and TM peaks produced by the AWG. Note again that the ranges for the core spacing and clad thickness represent possible values rather than a true specification. The circled points in Figure 3 indicate opportunities for reducing birefringence by a small amount in the base structure. Each should also be evaluated for their impact on optical performance to ensure that improving polarization independence does not degrade the device in some other ways.

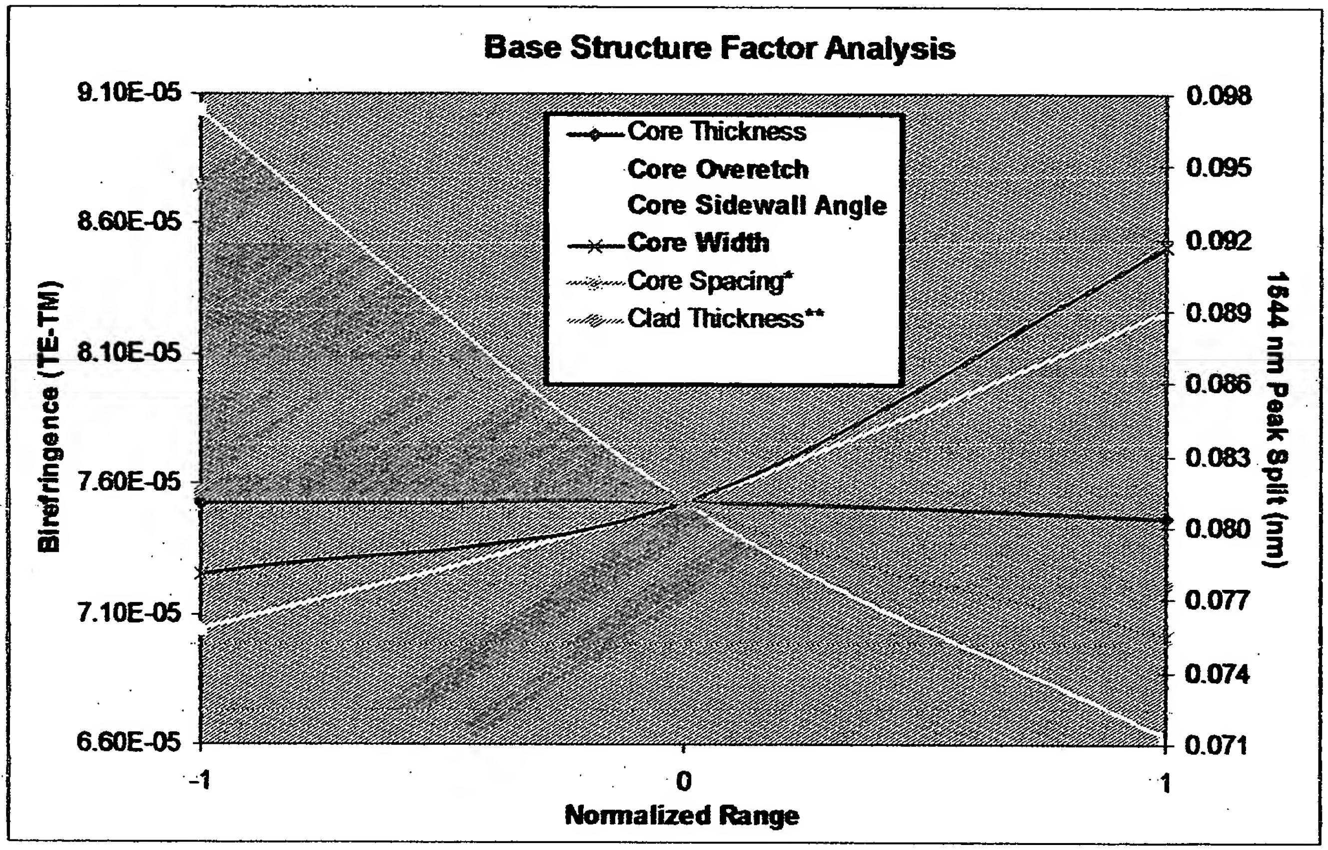

Figure 3: Simulated birefringence (or polarization peak split) for various single-factor adjustments to the nominal base AWG PLC structure. See Table 1 for corresponding parameter values.

AWG SRG Simulation Results

Simulations were run for the nominal SRG case and then for each end of the specification range shown in Table 2. The results are plotted in Figure 4 over a range of –1 to +1 indicating the normalized range for each variable. Birefringence values (RI shifts) are shown along with the expected split in TE and TM peaks produced by the AWG. Note that the results for alignment offset are not plotted with the nominal result at zero; instead, the nominal result is at –1, the +0.5 μm result at zero, and the +1.0 μm result at +1. The transparent blue region represents the target area where birefringence would be zero to within the accuracy of our best measurement tools (±3 pm).

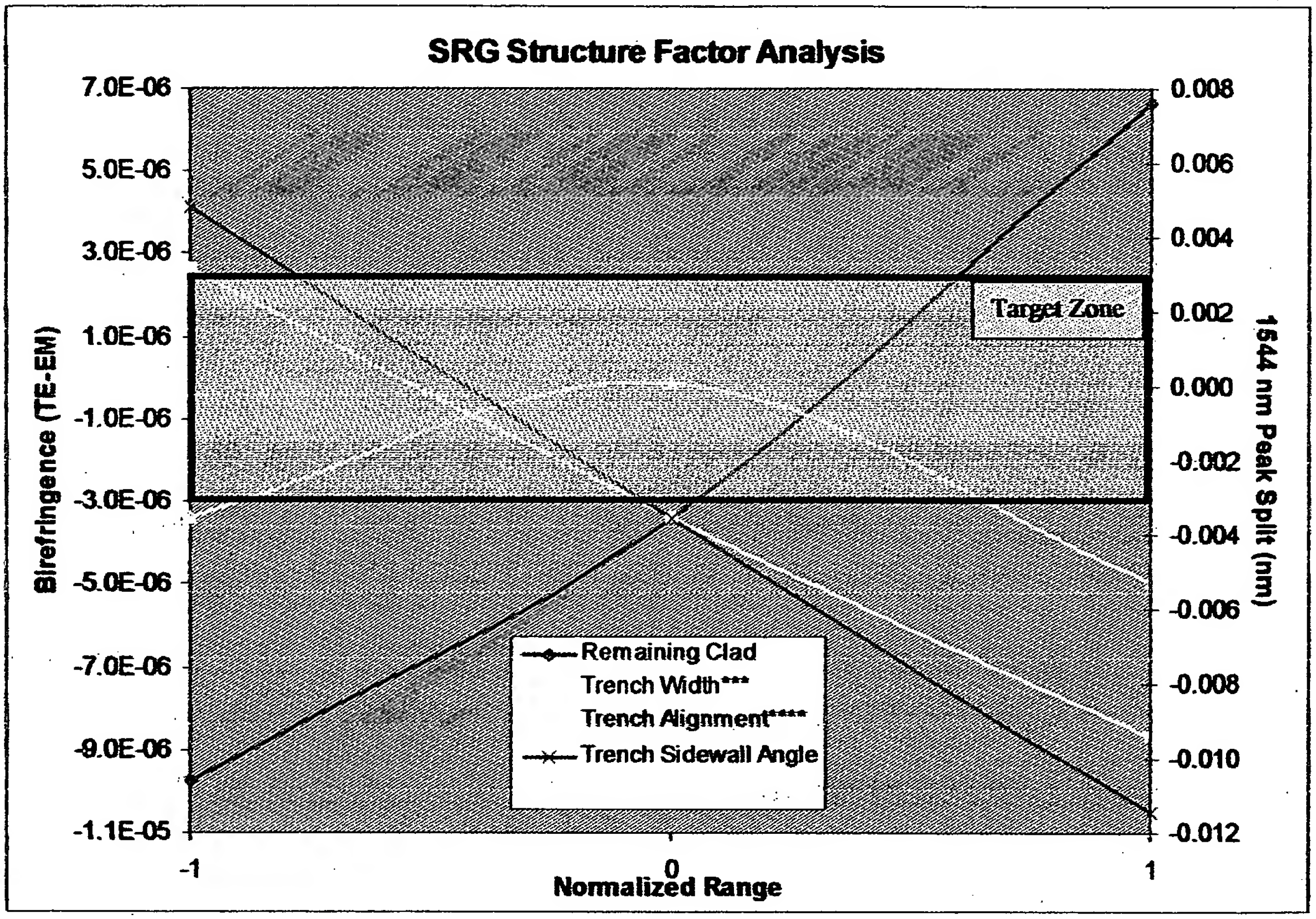

Figure 4: Simulated birefringence (or polarization peak split) for various single-factor adjustments to the nominal AWG SRG structure. See Table 2 for corresponding parameter values.